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EXAMINER	
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ART UNIT	PAPER NUMBER
2181	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/611,344	MACY ET AL.	
	Examiner	Art Unit	
	Benjamin P. Geib	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4,7-14,17-26,29,30,34-36,39-48,52 and 53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,7-14,17-26,29,30,34-36,39-48,52 and 53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
9/15/2006

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 4, 7-14, 17-26, 29, 30, 34-36, 39-48, 52, and 53 have been examined.

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as received on 07/03/2006.

Withdrawn Objections

3. Applicant, via amendment, has overcome the objection to claim 31 set forth in the previous Office Action. Consequently, this objection has been withdrawn by the examiner.

Withdrawn Rejections

4. Applicant, via amendment, has overcome the 35 U.S.C. § 112, second paragraph, rejections set forth in the previous Office Action. Consequently, these rejections have been withdrawn by the examiner.

Maintained Rejections

5. Applicant has failed to overcome the 35 U.S.C. 101 rejections set forth in the previous Office Action for claims 21-26, 29. Therefore, these rejections are respectfully maintained by the examiner and copied below for applicant's convenience. Further clarification of the rejection is now given. The claimed "machine-readable medium" is defined within the specification to include transmission media, including electro-magnetic signals (paragraphs 34 & 35, pages 9-10). Therefore, claim 21 claims a signal per se. An analysis of a signal per se done in accordance with the "Interim

Guidelines for Examination of Patent Applications for Patent Subject Matter Eligibility" concludes that a signal per se is not a process, machine, composition of matter, nor manufacture and, therefore, does not fall within any of the categories of patentable subject matter set forth in § 101. Therefore, claim 21 claims non-statutory subject matter.

6. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

7. The claimed invention is directed to non-statutory subject matter. Claim 21 refers to "machine readable medium", which is defined within the specification as including "any mechanism for storing or transmitting information in a form readable by a machine (e.g. a computer), but is not limited to, floppy disks, optical disks, ... a transmission over the Internet, electrical, optical, acoustical or other forms of propagated signals ..." (paragraphs 34 & 35, pages 9-10)." This definition includes transmission media, which is non-statutory subject matter.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1, 4, 7-14, 17-26, 29, 30, 34-36, 48, 52, and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rice et al., U.S. Patent No. 6,816,961, (Herein referred to as Rice) in view of Goodman & Miller, "A Programmer's View of Computer Architecture" (Herein referred to as Goodman).

10. Referring to claim 1, Rice has taught a method comprising:

responsive to receiving a single packed shuffle instruction *(byte swap instruction)* designating, with 3 bits, a first register *(first source register; Fig. 7, component 504)* storing a first operand having a set of L data elements *(source field; Fig. 7, component 512)* and designating, with 3 bits *(The first and second registers are each designated with six bits (column 6, lines 38-46). Since six bits includes three bits, the first and second registers are each designated with three bits.)*, a second register *(second source register; Fig. 7, component 508)* storing a second operand having a set of L control elements *(condition field; Fig. 7, component 700)*, wherein the first operand and second operand are of a same size and each of the L data elements and L control elements are of a same size *(column 6, lines 25-41; column 6, line 62 – column 7, line 6; column 7, lines 33-55)*, and

wherein each one of the L control elements is divided into three portions, the first portion being a flush to zero bit *(when the four most significant bits of the operation field (i.e. the third portion) are zeros then the least significant bit is a flush to zero bit; See Table 1)*, the second portion being a position selection field *(result field select value)* that is at least $\log_2 L$ bits wide and indicates a position of one of said L data elements,

and a third portion *(the four most significant bits of the operation field) (column 7, lines 50-56)*,

Rice does not disclose expressly that the flush to zero bit occupies the most significant bit of each control element.

At the time the invention was made, it would have been an obvious matter of design choice to a person of ordinary skill in the art to modify the operation field codes so that the code "10000" indicates the operation currently performed when the code is "00001" and vice versa *(doing so would make the flush to zero bit the most significant bit of each control element)* because Applicant has not disclosed that the flush to zero bit occupying the most significant bit of each control element provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with operation field of Rice because the operation field of Rice has a single flush to zero bit portion of the control element.

storing a resultant operand in a destination register having L resultant data elements of the same size as the L data elements and the L control elements *(column 7, lines 48-49; Fig. 7)*, wherein the value of each resultant data element is controlled by the position selection field of the L control elements in the same position as the resultant data element *(column 7, lines 53-55)*, and is either, the one of the L data elements designated by the position selection field of said control element if said control

element's flush to zero bit is not set; or a zero if said control element's flush to zero bit is set *(column 7, lines 57-67; Table I)*.

Rice does not disclose expressly that the destination register is the first register.

Goodman discloses using the first source register also as the destination register *(Goodman; two-address instruction format; page 199)*.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the method of Rice so that the first register specified by the instruction is also the destination register as taught by Goodman.

The suggestion/motivation for doing so would have been that the size of the instruction is reduced *(Goodman; 1st paragraph on page 200)*.

11. Referring to claim 4, Rice and Goodman have taught the method of claim 1 wherein said control element *(condition field)* is to designate a first operand data element *(source filed)* by a data element position number *(result field select value)* *(Rice; column 7, lines 49-55)*.

12. Referring to claim 7, Rice and Goodman have taught the method of claim 1 further comprising outputting a resultant data block comprising data that was shuffled from said first operand in response to said control elements of said second operand *(Rice; column 7, lines 32-42)*.

13. Referring to claim 8, Rice and Goodman have taught the method of claim 1 wherein each of said data elements comprises a byte of data *(Rice; column 6, line 62 – column 7, line 5; See Fig. 7, component 512)*.

14. Referring to claim 9, Rice and Goodman have taught the method of claim 8 wherein each of said control elements is a byte wide *(Rice; column 6, line 62 – column 7, line 5; See Fig. 7, component 700)*.

15. Referring to claim 10, Rice and Goodman have taught the method of claim 9 wherein L is 8 and wherein said first operand, said second operand, and said resultant are each comprised of 64-bit wide packed data *(Rice; column 6, lines 19-23; See Fig. 7, components 504, 508, and 524)*.

16. Referring to claim 11, Rice and Goodman have taught the method of claim 9 wherein L is 8 and wherein said first operand, said second operand, and said resultant are each comprised of 64-bit wide packed data *(column 6, lines 1-23)*.

Rice has not explicitly taught that L is 16 and wherein the first operand, second operand, and said resultant are each comprised of 128-bit wide packed data.

However, the Office takes Official Notice that 128-bit wide packed data operands are conventional and well known means of allowing an operation to be performed upon more byte sized elements at a time than a 64-bit wide packed data operand.

Therefore, it would have been obvious at the time the invention was made to one of ordinary skill in the art to modify the packed data operands of Rice to be 128-bit wide instead of 64-bit wide.

17. Referring to claim 12, Rice has taught an apparatus comprising:

an execution unit *(processing core; Fig. 1, component 12)* to execute a single packed shuffle instruction *(byte swap instruction)* designating, with 3 bits, a first register *(first source register; Fig. 7, component 504)* storing a first operand comprised of a set of L data elements *(source field; Fig. 7, component 512)* and designating, with 3 bits *(The first and second registers are each designated with six bits (column 6, lines 38-46). Since six bits includes three bits, the first and second registers are each designated with three bits.)*, a second register *(second source register; Fig. 7, component 508)* storing a second operand comprised of a set of L control elements *(condition field; Fig. 7, component 700)*, wherein the first operand and second operand are of a same size and each of the L data elements and L control elements are of a same size *(column 6, lines 25-41; column 6, line 62 – column 7, line 6; column 7, lines 33-55)*, and

wherein each one of the L control elements is divided into three portions, the first portion being a flush to zero bit *(when the four most significant bits of the operation field (i.e. the third portion) are zeros then the least significant bit is a flush to zero bit; See Table 1)*, the second portion being a position selection field *(result field select value)* that is at least $\log_2 L$ bits wide and indicates a position of one of said L data elements, and a third portion *(the four most significant bits of the operation field) (column 7, lines 50-56)*,

Rice does not disclose expressly that the flush to zero bit occupies the most significant bit of each control element.

At the time the invention was made, it would have been an obvious matter of design choice to a person of ordinary skill in the art to modify the operation

field codes so that the code "10000" indicates the operation currently performed when the code is "00001" and vice versa *(doing so would make the flush to zero bit the most significant bit of each control element)* because Applicant has not disclosed that the flush to zero bit occupying the most significant bit of each control element provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with operation field of Rice because the operation field of Rice has a single flush to zero bit portion of the control element.

said shuffle instruction to cause said execution unit to: store a resultant operand in a destination register having L resultant data elements of the same size as the L data elements and the L control elements *(column 7, lines 48-49; Fig. 7)*, wherein the value of each resultant data element is controlled by the position selection field of the L control elements in the same position as the resultant data element *(column 7, lines 53-55)*, and is either, a zero if said control element's flush to zero bit is true, otherwise the one of the L data elements designated by the position selection field of said individual control element *(column 7, lines 57-67; Table I)*.

Rice does not disclose expressly that the destination register is the first register.

Goodman discloses using the first source register also as the destination register *(Goodman; two-address instruction format; page 199)*.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the method of Rice so that the first register specified by the instruction is also the destination register as taught by Goodman.

The suggestion/motivation for doing so would have been that the size of the instruction is reduced *(Goodman; 1st paragraph on page 200)*.

18. Referring to claim 13, Rice and Goodman have taught the apparatus of claim 12 wherein each of said L control elements occupies a position in said second operand and is associated with a similarly located data element position in a resultant *(Rice; See Fig. 5; column 6, line 62 – column 7, line 6)*.

19. Referring to claim 14, given the similarities between claim 4 and claim 14 the arguments as stated for the rejection of claim 4 also apply to claim 14.

20. Referring to claim 17, Rice and Goodman have taught the apparatus of claim 12 wherein said shuffle instruction is to further cause said execution unit to generate a resultant having L data element positions that have been filled based on said set of L control elements *(Rice; column 7, lines 32-42)*.

21. Referring to claim 18, given the similarities between claim 9 and claim 18 the arguments as stated for the rejection of claim 9 also apply to claim 18.

22. Referring to claim 19, given the similarities between claim 10 and claim 19 the arguments as stated for the rejection of claim 10 also apply to claim 19.

23. Referring to claim 20, given the similarities between claim 11 and claim 20 the arguments as stated for the rejection of claim 11 also apply to claim 20.

24. Referring to claim 21, given the similarities between claim 1 and claim 21 the arguments as stated for the rejection of claim 1 also apply to claim 21.

25. Referring to claim 22, Rice and Goodman have taught the article of manufacture of claim 21.

Rice has not explicitly taught that said data stored by said machine readable medium represents an integrated circuit design, which when fabricated performs said predetermined function in response to a single instruction.

However, the Office take Official Notice that a Hardware Description Language (HDL) data representation of an integrated circuit design, stored by a machine readable medium, that when fabricated performs a predetermined function in response to single instruction is a conventional and well known means to store an integrated circuit design.

Therefore, It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify the data stored on a machine readable medium of Rice to be a Hardware Description Language data representation of an integrated circuit design on a machine readable medium that when fabricated performs a predetermined function in response to a single instruction.

26. Referring to claim 23, given the similarities between claim 17 and claim 23 the arguments as stated for the rejection of claim 17 also apply to claim 23.

27. Referring to claim 24, given the similarities between claim 2 and claim 24 the arguments as stated for the rejection of claim 2 also apply to claim 24.

28. Referring to claim 25, given the similarities between claim 4 and claim 25 the arguments as stated for the rejection of claim 4 also apply to claim 25

29. Referring to claim 26, given the similarities between claim 8 and claim 26 the arguments as stated for the rejection of claim 8 also apply to claim 26.

30. Referring to claim 29, Rice and Goodman have taught the article of manufacture of claim 21 wherein said data stored by said machine readable medium *(Rice; memory; column 3, lines 1-26)* represents a computer instruction, which, if executed by a machine, causes said machine to perform said predetermined function *(Rice; column 6, lines 25-53).*

31. Referring to claim 30, given the similarities between claim 1 and claim 30 the arguments as stated for the rejection of claim 1 also apply to claim 30. The additional limitation in claim 30 of "and, wherein each of said L masks occupies a particular position in said second operand and is associated with a similarly located data element position in a resultant operand" is supported at column 6, line 62 – column 7, line 6 and in Fig. 5 of Rice. It is noted that the "masks" of claim 30 correspond to the "control elements" of claim 1.

32. Referring to claim 34, Rice and Goodman have taught the method of claim 30 wherein said first operand, said second operand, and said resultant are each comprised of 64-bit wide packed data (column 6, lines 19-23; See Fig. 7, components 504, 508, and 524).

33. Referring to claim 35, given the similarities between claim 11 and claim 35 the arguments as stated for the rejection of claim 11 also apply to claim 35.

34. Referring to claim 36, given the similarities between claim 30 and claim 36 the arguments as stated for the rejection of claim 30 also apply to claim 36.

35. Referring to claim 48, Rice has taught a system comprising:

a memory to store data and instructions *(memory; Fig. 1, component 14)*;

a processor *(processing core; Fig. 1, component 12)* coupled to said memory on a bus *(See Fig. 1)*, said processor operable to perform a shuffle operation *(byte swap instruction; column 6, lines 25-54)*, said processor comprising:

a bus unit *(See Fig. 1)* to receive a single packed shuffle instruction, from said memory, said instruction to designate, with 3 bits, a first register *(first source register; Fig. 5, component 504)* storing L data elements *(source fields; Fig. 5, component 512)* from a first operand, and to designate, with three bits *(The first and second registers are each designated with six bits (column 6, lines 38-46). Since six bits includes three bits, the first and second registers are each designated with three bits.)*, L shuffle control elements *(condition fields; Fig. 7, component 700)* from a second operand *(second source register; Fig. 7, component 508)*, wherein the first operand and second operand are of same size and each of the L data elements and L control elements are of a same size *(column 6, lines 25-41; column 6, line 62 – column 7, line 6; column 7, lines 33-55)*, and

wherein each one of the L control elements is divided into three portions, the first portion being a flush to zero bit *(when the four most significant bits of the operation field (i.e. the third portion) are zeros then the least significant bit is a flush to zero bit; See Table 1)*, the second portion being a position selection field *(result field select value)* that is at least $\log_2 L$ bits wide and indicates a position of

one of said L data elements, and a third portion *(the four most significant bits of the operation field) (column 7, lines 50-56)*,

Rice does not disclose expressly that the flush to zero bit occupies the most significant bit of each control element.

At the time the invention was made, it would have been an obvious matter of design choice to a person of ordinary skill in the art to modify the operation field codes so that the code "10000" indicates the operation currently performed when the code is "00001" and vice versa *(doing so would make the flush to zero bit the most significant bit of each control element)* because Applicant has not disclosed that the flush to zero bit occupying the most significant bit of each control element provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with operation field of Rice because the operation field of Rice has a single flush to zero bit portion of the control element.

an execution unit *(processing path; Fig. 2, component 56)* coupled to said bus unit, said execution unit to execute said single packed shuffle instruction *(column 4, lines 46-61)*, said single packed shuffle instruction to cause said execution unit to:

store a resultant operand in a destination register having L resultant data elements of the same size as the L data elements and the L control elements

(column 7, lines 48-49; Fig. 7), wherein the value of each resultant data element is controlled by the position selection field of the L control elements in the same position as the resultant data element *(column 7, lines 53-55)*, and is either,

the one of the L data elements designated by the position selection field of said control element if said control element's flush to zero bit is not set; or a zero if said control element's flush to zero bit is set *(column 7, lines 57-67; Table I)*.

Rice does not disclose expressly that the destination register is the first register.

Goodman discloses using the first source register also as the destination register *(Goodman; two-address instruction format; page 199)*.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the method of Rice so that the first register specified by the instruction is also the destination register as taught by Goodman.

The suggestion/motivation for doing so would have been that the size of the instruction is reduced *(Goodman; 1st paragraph on page 200)*.

36. Referring to claim 52, Rice and Goodman have taught the system of claim 48 wherein each data element *(source fields; Fig. 7, component 512)* is a byte wide, each shuffle command element *(condition fields; Fig. 7, component 700)* is a byte wide, and L is 8 *(See Fig. 7)*.

37. Referring to claim 53, Rice and Goodman have taught the system of claim 48 wherein said first operand *(first source register; Fig. 7, component 504)* is 64 bits long

and said second operand *(second source register; Fig. 7, component 508)* is 64 bits long (See Fig. 7).

38. Claims 39-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rice in view of Goodman, and further in view of Hoyle et al., U.S. Patent Application Publication 2005/0188182 (Herein referred to as Hoyle).

39. Referring to claim 39, Rice has taught an apparatus comprising:

a first memory location *(first source register; Fig. 5, component 504)* to store a plurality of source data elements *(source fields; Fig. 5, component 512)*;

a second memory location *(second source register; Fig. 7, component 508)* to store a plurality of control elements *(condition fields; Fig. 7, component 700)*, each of said control elements to correspond to a resultant data element position *(result field; Fig. 7, component 528) (column 6, line 62 – column 7, line 2; See Fig. 7)*, and wherein each one of said control elements is divided into three portions, the first portion being a flush to zero bit *(when the four most significant bits of the operation field (i.e. the third portion) are zeros then the least significant bit is a flush to zero bit; See Table 1)*, the second portion being a position selection field *(result field select value)* that is at least $\log_2 L$ bits wide and indicates a postion of one of said L data elements, and a third portion *(the four most significant bits of the operation field) (column 7, lines 50-56)*;

Rice does not disclose expressly that the flush to zero bit occupies the most significant bit of each control element.

At the time the invention was made, it would have been an obvious matter of design choice to a person of ordinary skill in the art to modify the operation field codes so that the code "10000" indicates the operation currently performed when the code is "00001" and vice versa *(doing so would make the flush to zero bit the most significant bit of each control element)* because Applicant has not disclosed that the flush to zero bit occupying the most significant bit of each control element provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with operation field of Rice because the operation field of Rice has a single flush to zero bit portion of the control element.

control logic *(logic wires from second source register; See Fig. 7)* coupled to said first memory location and said second memory location *(second source register)*, said control logic in response to the receipt of a single packed shuffle instruction designating, with three bits *(The first and second memory locations are each designated with six bits (column 6, lines 38-46). Since six bits includes three bits, the first and second memory locations are each designated with three bits.)*, a first memory location storing a first operand having a set of L data elements and designating a second memory location storing a second operand having a set of L control elements, wherein the first operand and the second operand are of a same size and each of the L data elements and L control elements are of a same size, to generate a plurality of selection signals and a plurality of flush to zero signals, a zero signal generated when a control element's flush

to zero bit is set *(column 6, lines 25-41; column 6, line 62 – column 7, line 6; column 7, lines 33-55)*;

a first plurality of multiplexers *(multiplexers; Fig. 7)* coupled to said first memory location *(second source register)* and said plurality of selection signals (*logic wires from second source register)*, each of said first plurality of multiplexers to store a resultant operand in a destination memory location having L resultant data elements of the same size as the L data elements and the L control elements, wherein the value of each resultant data element is controlled by the position selection signal of the L control elements in the same position as the resultant data element *(column 7, lines 43-56)*, and is the one of the L data elements *(source fields)* for a specific resultant data element position *(result field)* in response to a selection signal corresponding to said specific resultant data element position *(column 7, lines 2-10, 33-49)*; and

Rice does not disclose expressly that the destination memory location is the first memory location.

Goodman discloses using the first source register also as the destination register *(Goodman; two-address instruction format; page 199)*.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the method of Rice so that the first memory location specified by the instruction is also the destination memory location as taught by Goodman.

The suggestion/motivation for doing so would have been that the size of the instruction is reduced *(Goodman; 1st paragraph on page 200)*.

a processing component *(operand processor; Fig. 7, component 704)* coupled to said first plurality of multiplexers and to said plurality of flush to zero signals, each of said processing components associated with a specific resultant data element position *(result field)*, each of said processing components to output a zero if its flush to zero signal is active or to output a data element shuffled for that specific resultant data element position *(column 7, lines 43-67; Table I)*.

Rice has not explicitly taught that the processing components are multiplexers.

Hoyle also taught a system for intermingling/swapping bytes that uses a plurality of multiplexers to select between zero and a shuffled data element *(See Fig. 7c, paragraphs 94-96, 119)*.

It would have obvious at the time the invention was made to one of ordinary skill in the art to replace the processing component *(operand processor)* of Rice with the multiplexer of Hoyle since one of ordinary skill in the art would have recognized that doing so would allow a simpler, and possibly faster, means for selection between zero and a shuffled data element.

40. Referring to claim 40, Rice, Goodman, and Hoyle have taught the apparatus of claim 39 wherein said plurality of source data elements *(source fields)* is a first packed data operand *(Rice; column 6, lines 38-41; column 6, line 62 – column 7, line 5)*.

41. Referring to claim 41, Rice, Goodman, and Hoyle have taught the apparatus of claim 40 where said plurality of control elements *(condition fields)* is a second packed data operand *(Rice; column 6, lines 38-41; column 6, line 62 – column 7, line 5)*.

42. Referring to claim 42, Rice, Goodman, and Hoyle have taught the apparatus of claim 40 wherein said first and second memory locations are a single instruction multiple data registers *(Rice; column 5, lines 58-67)*.

43. Referring to claim 43, Rice, Goodman, and Hoyle have taught the apparatus of claim 42 wherein:

said first packed operand is 64 bits long and each of said source data elements is a byte wide *(Rice; column 6, lines 19-22; column 6, line 62 – column 7, line 5)*; and

said second packed operand is 64 bits long and each of said control elements is a byte wide *(Rice; column 6, lines 19-22; column 6, line 62 – column 7, line 5)*.

44. Referring to claim 44, given the similarities between claim 11 and claim 44 the arguments as stated for the rejection of claim 11 also apply to claim 44.

45. Referring to claim 45, Rice has taught an apparatus comprising:

control logic *(logic wires from second source register; See Fig. 7)* to receive a single packed shuffle instruction designating, with three bits, a first memory location *(first source register; Fig. 7, component 504)* storing a first operand having a set of M data elements *(source fields; Fig. 7, component 512)* and designating, with three bits *(The first and second registers are each designated with six bits (column 6, lines 38-46). Since six bits includes three bits, the first and second registers are each designated with three bits.)*, a second memory location *(second source register; Fig. 7, component 508)* storing a second operand having a set of L shuffle masks *(condition fields; Fig. 7, component 700)*, wherein each of the M data elements and L shuffle masks are of a

same size *(column 6, lines 25-41; column 6, line 62 – column 7, line 6; column 7, lines 33-55)*, and

wherein each one of the L shuffle masks is divided into three portions, the first portion being a flush to zero bit *(when the four most significant bits of the operation field (i.e. the third portion) are zeros then the least significant bit is a flush to zero bit; See Table 1)*, the second portion being a position selection field *(result field select value)* that is at least $\log_2 L$ bits wide and indicates a postion of one of said L data elements, and a third portion *(the four most significant bits of the operation field) (column 7, lines 50-56)*;

Rice does not disclose expressly that the flush to zero bit occupies the most significant bit of each shuffle mask.

At the time the invention was made, it would have been an obvious matter of design choice to a person of ordinary skill in the art to modify the operation field codes so that the code "10000" indicates the operation currently performed when the code is "00001" and vice versa *(doing so would make the flush to zero bit the most significant bit of each shuffle mask)* because Applicant has not disclosed that the flush to zero bit occupying the most significant bit of each shuffle mask provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with operation field of Rice because the operation field of Rice has a single flush to zero bit portion of the shuffle mask.

wherein each shuffle mask is associated with a unique resultant data element position *(result field; Fig. 7, component 528)* controlled by the position selection field of said shuffle mask, said control logic to provide a select signal *(result field select value output)* and a flush to zero signal *(operation field output)* for each resultant data element position; and *(column 7, lines 2-10, 50-67; See Fig. 7)*

a set of L processing components *(operand processors)* coupled to said control logic, wherein each processing component is also associated with a unique resultant data element position *(result field)*, each processing component to output to a destination memory location either, a zero if said shuffle mask's flush to zero signal is active or the one of the M data elements designated by the select signal of said shuffle mask if said shuffle mask's flush to zero signal is inactive *(column 7, lines 43-67; Table I)*.

Rice does not disclose expressly that the destination memory location is the first memory location.

Goodman discloses using the first source register also as the destination register *(Goodman; two-address instruction format; page 199)*.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the method of Rice so that the first memory location specified by the instruction is also the destination memory location as taught by Goodman.

The suggestion/motivation for doing so would have been that the size of the instruction is reduced *(Goodman; 1st paragraph on page 200)*.

Rice has not explicitly taught that the processing components are multiplexers.

Hoyle also taught a system for intermingling/swapping bytes that uses a plurality of multiplexers to select between zero and a shuffled data element *(See Fig. 7c, paragraphs 94-96, 119)*.

It would have obvious at the time the invention was made to one of ordinary skill in the art to replace the processing component *(operand processor)* of Rice with the multiplexer of Hoyle since one of ordinary skill in the art would have recognized that doing so would allow a simpler, and possibly faster, means for selection between zero and a shuffled data element.

46. Referring to claim 46, Rice, Goodman, and Hoyle have taught the apparatus of claim 45 further comprising a register *(destination register; Fig. 7, component 524)* with L unique data element positions *(result field; Fig. 7, component 528)*, each data element position to hold an output from its associated multiplexer *(column 7, lines 33-49; See Fig. 7)*.

47. Referring to claim 47, given the similarities between claim 11 and claim 47 the arguments as stated for the rejection of claim 11 also apply to claim 47.

Response to Arguments

48. Applicant's arguments filed on 07/03/2006 have been fully considered but they are considered moot in view of the new rejections above, which were necessitated by the amendments to the claims.

Conclusion

49. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

50. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Benjamin P. Geib whose telephone number is (571) 272-8628. The examiner can normally be reached on Mon-Fri 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Benjamin P Geib
Examiner
Art Unit 2181

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9/15/2006